

A 1.7mA Low Noise Amplifier with Integrated Bypass Switch for Wireless 0.05-6 GHz Portable Applications

Henrik Morkner, Mike Frank, Shun Yajima

Agilent Technologies WSD R&D
39201 Cherry Street, MS 830 NK10
Newark, California, 94560

ABSTRACT

An ultra low current low noise amplifier with an integrated bypass switch has been developed using PHEMT technology. The LNA/Sw uses only 1.7 mA when powered and less than 1 μ A when bypassed. It is usable from 50 MHz to 6 GHz. This enables portable systems such as Bluetooth, Home RF, PDAs, wireless LANs. The LNA provides 15 dB gain, 1.8 dB noise figure with 50 Ω load at the output and Γ_{opt} at the input. Bypass mode provides 5 dB insertion loss into the same I/O match. The LNA and bypass switch with associated control circuitry are integrated into a single RFIC and housed in the miniature SOT package. This LNA/Sw provides lower current and easier usage with comparable NF, Gain, and bandwidth than previously reported products.[2]

INTRODUCTION

Current draw is the defining factor for battery life in any portable wireless application. This is especially true for the receiver LNA(Low Noise Amplifier) since it must be powered continuously in order for the handset to "listen" for incoming signals. The LNA must be extremely current efficient yet provide the gain, noise figure and linearity that any portable wireless system demands.

A modern portable receiver does not need the LNA gain when an incoming signal is strong. For instance a typical intelligent receiver may only need the LNA 20% of the time. In this case, it is often advantageous to bypass the LNA to increase its efficiency and dynamic range of the handset. Efficient bypass networks utilize voltage controlled FETs that increase system linearity and draw near zero current.

The LNA in this paper powered to 1.7mA provides the gain and noise figure needed in a typical portable system. When the bypass mode is activated, the LNA section is automatically powered down, creating an effective current of zero. If powered 20% of the on time, the average current of the LNA/Sw

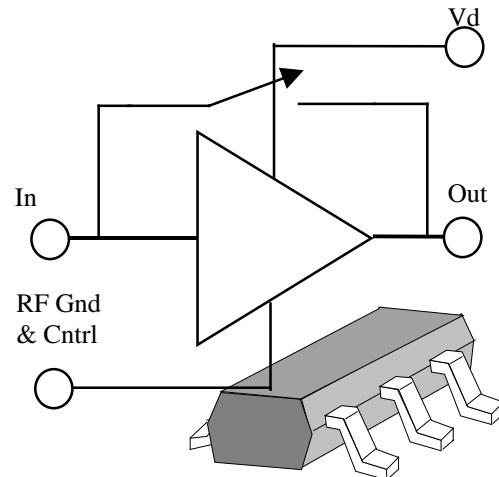


Figure 1. Low noise amp. with bypass switch.

is only 0.34 mA. This is more efficient than solutions published or available on the market. In addition, this solution is a single low cost RFIC in a miniature package that provides all RF performance needs. It can be used in GPS, Bluetooth, Home RF, PDAs, wireless LANs. It is operational in all ISM frequencies at 800MHz, 2.4GHz and 5.8 GHz applications.

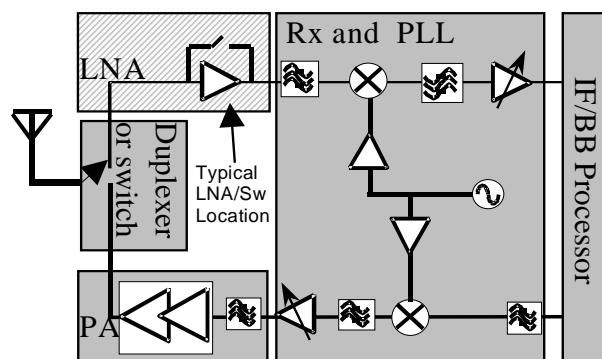


Figure 2. LNA/Sw in a typical mobile receiver.

TYPICAL USAGE

One typical mobile receiver application of the LNA/Sw is shown in Figure 2 for portable Bluetooth and Home RF wireless technology. These radio operates on the globally-available unlicensed radio band, 2.45 GHz, and support data speeds of up to 721 Kbps, as well as three voice channels. A Bluetooth radio is certainly going to be dominated by highly integrated CMOS or BiCMOS ICs. However, the sensitivity of the receiver has to be in excess of -90 dBm and even better if superior range or noise reduction is needed. This certainly taxes the capabilities of modern CMOS or even SiGe technology. In addition, any signal leakage through the switch or duplexer can easily saturate a LNA if it does not have the capability to be bypassed or provide sufficient linearity.

One solution is to add a separate LNA/Sw to the radio ASIC chip/chip set. This allows the ASIC designer to concentrate on low-voltage, low-power, and low-cost signal processing and not low noise RF performance. A sub 2 dB NF and 15 dB first stage gain can meet sensitivity requirements up to -100 dBm, vastly improving receiver performance with a low current cost of 1.7mA. When the additional sensitivity is not needed, the portable receiver can actively shut the LNA and activate the bypass switch. This now requires virtually no current. The LNA/Sw is small (4 mm sq) and low cost (sub \$0.50) as to keep the portable receiver viable.

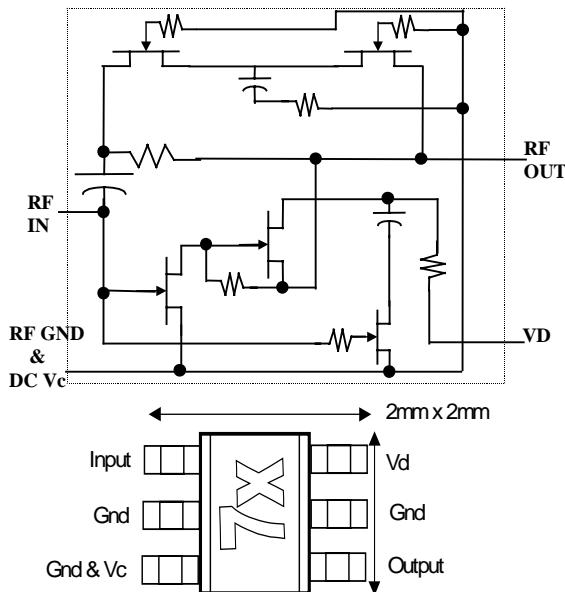


Figure 3. LNA/Sw design

MONOLITHIC LNA/Sw DESIGN

The challenge of this design was to make a low noise amplifier with sufficient gain, noise figure and I/O match. The basic PHEMT FETs provide sufficient gain and noise figure to meet the requirements even at these low current levels. The difficulty lies in matching very low current devices, that are essentially high impedance networks, to $50\ \Omega$.

The solution to this problem is to use a two stage amplifier. The first stage consists of a traditional common source FET gain stage. The second stage is a source follower stage that acts as an active impedance matching network. The drain of the second stage is bypassed to complete the circuit. Since the source follower stage does not rotate the phase 180 degrees, it can be directly fed back to the input. This feedback greatly reduces the input Γ magnitude, partially matching the input to $50\ \Omega$. Only a small series input inductor is needed externally to complete the match, which is left to the user, thus avoiding to impact on the wide band performance of the RFIC.

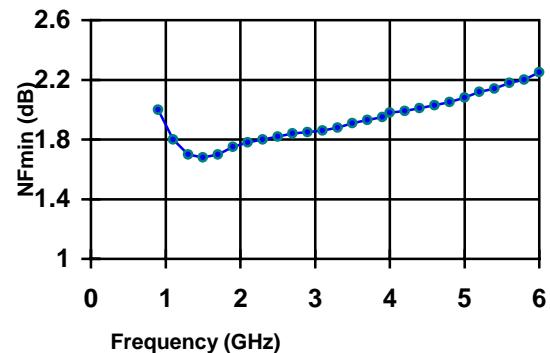


Figure 4. Minimum Noise Figure in LNA mode

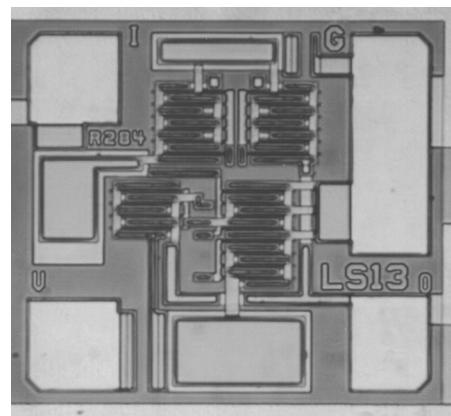


Figure 5. LNA/Sw as fabricated

Since the output is at $50\ \Omega$ impedance, noise contribution of feedback is minimal. The supply voltage is split between the two stages, allowing the current to be reused. This does cut down the FET Drain-source voltage, but PHEMT devices are comfortable with voltages in the 1 to 2 Volt range.

To incorporate a bypass switching topology into the LNA, three PHEMT FETs are employed as cold channel voltage controlled resistors. Operation of the LNA and switch is covered in patent 6,118,338 "Low Noise Amplifier Circuit with an Isolating Switch Topology", inventors Michael L. Frank and Henrik Morkner. During LNA operation the series bypass FETs have the gate-source voltage pulled beyond pinch-off and thus are in a "off" state. The shunt FET has all three terminals at the same potential, thus is "on" and provides LNA Drain ground. When the DC current is cut from the device, the series FET terminals are pulled to the same potential through an external 30K pull-up resistor and thus turn "on". The shunt FETs Drain and Source terminals pull up to V_d yet the gates are tied externally through a resistor to ground, thus turn "off". Between the series FETs is a RC interstage network allows proper isolation and minimizes phase change.

Figure 3 shows a simplified schematic of the RFIC as built and how it is packaged for small size, high volume, low cost applications. Figure 4 shows measured F_{min} of the LNA/Sw in the LNA mode.

DEVICE AND FABRICATION

The devices used in this monolithic design were pseudomorphic high electron mobility transistor (PHEMT) structures built using molecular beam epitaxy (MBE) material growth. Gate lengths are approximately $1/2\ \mu\text{m}$. All layers are placed on the 4-inch wafers using a stepper. The result is a process with typical F_T of 35 GHz and able to operate at low voltage and provide low noise figure.

Figure 5 shows the compact size of the design. Die size is only 0.37 mm per side, allowing it to fit easily in the miniature SC-70 package.

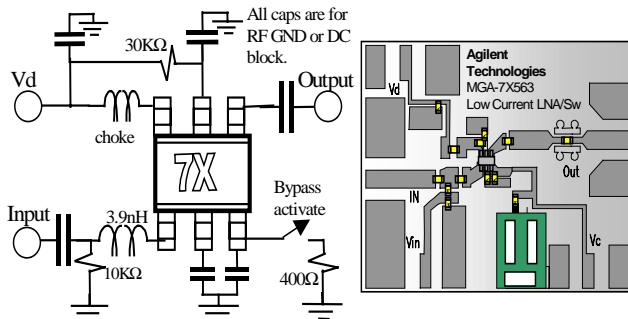


Fig 6. 2.4 GHz LNA/Sw demonstration circuit.

MEASURED PERFORMANCE

Parameter	LNA Active	Bypass
Output P1dB	-9 dBm	+18 dBm
Output IP3	+1 dBm	+30 dBm
I _{dc}	1.7 mA	< 5 μA
Gain	15 dB	-4.5 dB
Input Return Loss	-12 dB	-9.8 dB
Output Return Loss	-15 dB	-18 dB

Table 1. LNA/Sw performance at 2.4 GHz

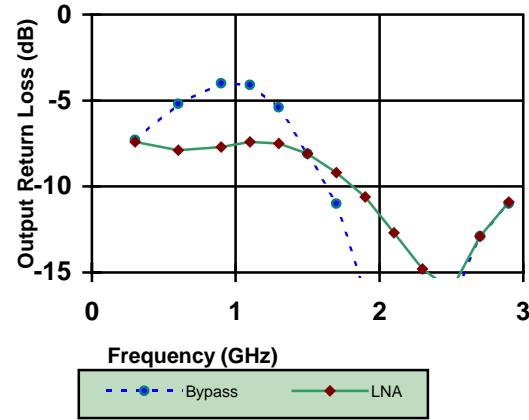
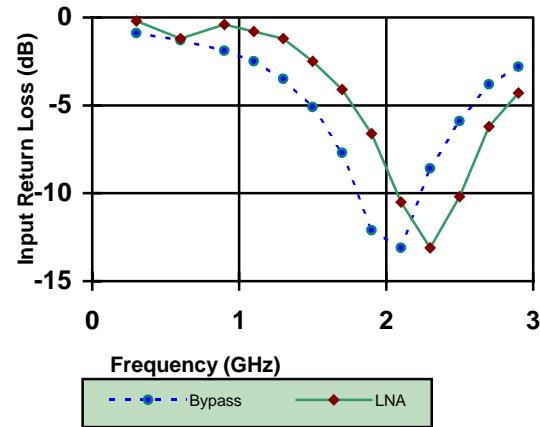
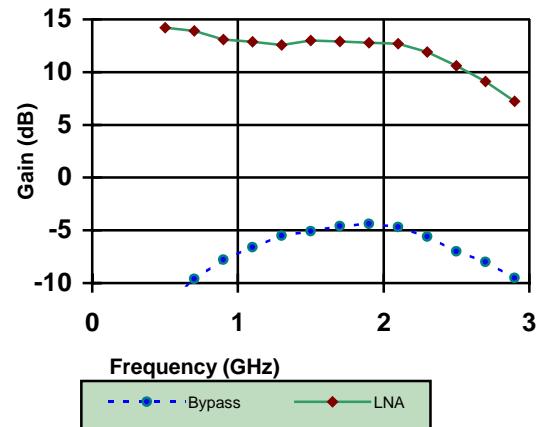


Fig 7 a,b,c, Demo board 2.4 GHz performance

Minimal RF matching is required for the MMIC. The output is at $50\ \Omega$. Measured 2.4 GHz minimum noise input Γ typically has a magnitude less than 0.6 to give a 1.82 dB NF with 14.9 dB of associated gain. It can be matched with a simple series inductor.

A 2.4 GHz demonstration board for a SC70 packaged LNA/Sw is shown in Figure 6. Measured data shown in Figure 7 shows operation at LNA and bypass modes. A gain of 13 dB or insertion loss of $-4.5\ \text{dB}$ are measured. The in and out return loss are maintained better than $-10\ \text{dB}$ over all modes, proving the mitigative network is functional. The same board with the input match optimized for 900 MHz provides 18 dB gain with the same I/O return loss. At 5.8 GHz over 10dB gain is achievable with 2.1 dB noise figure and good I/O match.

It is important for the portable receiver that mismatch is minimized when going from LNA to bypass mode since some systems can have filters on both sides of the RFIC. Mis-match into filters can causes serious system gain ripple and degrade receiver performance. The RFIC is matched with Γ_{opt} impedance at the input and $50\ \Omega$ at the output, providing excellent match and performance for the LNA mode. When the bypass mode is activated, not only is the LNA shut down and the incoming signal re-routed, the signal is routed through a patented mitigate network [10]. This network provides a low reflection load, even though the LNA Γ_{opt} is still present at the RFIC and reduces system gain ripple.

CONCLUSION

The LNA/Sw described in this paper integrates a two stage amplifier where the second stage provides an active match so the output of the RFIC is $50\ \Omega$ across the entire band. The LNA minimum noise figure is 1.8 dB at 2.4 GHz with an associated gain of 14.9 dB. A limited amount of internal feedback is used to ensure unconditional stability over frequency and temperature of this RFIC. The feedback also partially matches the input so only a small value series inductor is needed for a specific frequency Γ_{opt} or S_{11}^* match.

The LNA/Sw RFIC also provides an integrated bypass switch and bias control circuit. When current to the LNA is shut down, the bypass function is automatically activated. In this mode the insertion loss through the RFIC is less than 5dB, while input and output match is maintained at $50\ \Omega$, even with the LNA input matching structure still applied. The control circuitry draws near zero current.

A low current LNA with integrated bypass switch has been demonstrated for battery operated portable receiver RF applications. Frequency of operation is

50MHz to 6 GHz, which includes the globally-available unlicensed radio bands. The RFIC is housed in a low cost, small size, SOT package. The LNA/Sw operates on a single 3V supply and uses only 1.7 mA in LNA mode, 1 uA when in bypass mode. The LNA mode NF has been measured at 1.8 dB with associated gain of 15 dB at 2.4 GHz. The bypass mode insertion loss is less than 5 dB. I/O match is maintained at $50\ \Omega$ over all modes. To the best of our knowledge, this is the lowest current and best performance solution available in research or commercial form for modern portable receiver usage.

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